**Pre-Lab:**

1. Design a Common Gate stage with a gain of 5 and an input impedance = 50 Ohms. Assume Vov = 0.1 V, VDD = 1.8V. Assume a voltage divider biasing, this means you need to find RS, RD, R1 and R2 as well as the (W/L) ratio.
2. Design a Source Follower with a gain of 0.6 for an RL = 100 Ohms, and an Input impedance of 100KOhms. Assume a simple biasing structure using an RG and a VDD = 1.8V.

*Assume kp = 100 µA/V2, VTH = 0.4V, and Lambda = 0*

***Task #1:***

1. Implement the CG stage in pre-lab step 1 using LTSpice, Run a .op analysis to verify your biasing.
2. Use a test voltage of 1mV and a 100 Hz frequency and show that the gain is indeed 5, this can be done by comparing the input test voltage with the output voltage. In addition to that, notice the match between the input and the output phase. Justify the gain mathematically. (Apply the same LTspice directives in Lab 5)
3. Verify that the input impedance = 50 Ohms. This should be done by applying a test voltage and measuring the test current. (Apply the same LTspice directives in Lab 5)
4. Connect a 100 Ohms load to the output of the CG stage and notice the drop in the voltage gain. Justify this drop mathematically.

***Task#2:***

1. Implement the source follower in pre-lab step 2 using LTspice. Run a .op analysis to verify your biasing.
2. Show that the voltage gain is indeed 0.6 by connecting the test source you used in task#1 step b. Justify your observation mathematically.
3. Cascade the CG and SF using LTspice and show through simulation that the drop in the voltage gain in task#1 step d is remedied.
4. The overall gain for cascading two stages is the (Av for the CG \* Av for the SF). Notice that the input voltage for the SF stage is not exactly Av for the CG \* Vin, justify this observation mathematically?
5. Justify the gain in task#2 step h mathematically.